It is our great pleasure to welcome you to the two joint conferences of EUROMICRO: the 15th EUROMICRO Digital Systems Design (DSD2012) and the 38th EUROMICRO Software Engineering and Advanced Applications (SEAA2012). The unique integration of these two high quality conferences provides an opportunity for interdisciplinary research to be presented and enables scientist to observe connections as well as collaboration opportunities among diverse fields.

We are honored to host the two traditional conferences of the field in an historical town Cesme, (meaning fountain, historical name Cyssus) established almost 3000 years ago. Cesme is at the western-most end of Turkey and close to Izmir which is one of the oldest settlements of the Mediterranean basin and the birth place of Homer. We hope the region will reward SEAA2012 and DSD2012 participants with its history, blue waters, meltemi winds and delicious Aegean food while we discuss research results and innovative new ideas.

This year the quantity of submissions was beyond our expectations. Program committees of SEAA and DSD have done an excellent work of reviewing and selecting the papers, posters and tutorials. We would like to first thank all the authors for their high quality research and their decision to present their work in Euromicro. We would like to thank the program chairs, Smail Nair (DSD), Vittorio Cortellessa and Henry Muccini (SEAA), the track chairs, the program committees and associated reviewers for selecting high quality work and providing significant feedback to the authors.

We also would like to take this opportunity to thank our publicity chair Oktay Turetken, proceedings chair Amund Skavhaung, sponsor chair Aysu Betin Can, the teaching assistants, Mahir Kaya, Ozge Gurbuz, Erdir Ungan, Baris Ozkan, Gokcen Yilmaz, Mina Babi, Buket Aran of the Middle East Technical University, Informatics Institute, Ozden Hanoglu, graphics designer, and Cagla Ozer, the representative of the organization agency.

We hope the conference in Cesme will become a fountain to provide a wonderful scientific experience in a traditional Turkish hospitality.

Altan Kocyigit
Organization Chair

Onur Demirors
General Chair

Euromicro DSD 2012 and
Euromicro SEAA 2012
38th Euromicro Conference on Software Engineering and Advanced Applications (SEAA’2012) and 15th Euromicro Conference on Digital System Design (DSD’2012) will be held in Çeşme, İzmir. Çeşme is surrounded by the Aegean Sea in three sides at the very western end of Urla Peninsula, and is neighbor of the Sakız (Chios) Island (Greece).

Organizer of the conference is Middle East Technical University (METU). METU has 40 undergraduate programs within 5 faculties. Additionally, there are 5 Graduate Schools with 100 masters and 66 doctorate programs and a “School of Foreign Languages” which includes the English Preparatory Department. 14 undergraduate programs and 2 graduate programs are offered in connection with METU Northern Cyprus Campus. METU has strong teaching, research and social services for its students so that research, creativity and self-development can be fostered.
Alexander Egyed
Model-Driven Engineering and the Impact of a Change

Abstract

Design models describe different viewpoints of a software system — separating functionality, from structure, behavior, or usage. While these models are meant to be separate in their description, they are nonetheless related by manifold dependencies. After all, they describe the same system. Yet, this network of dependencies is also the most significant obstacle to model-driven engineering. It is the root cause for failure to propagate changes correctly and completely. Although change propagation as a whole is a daunting challenge to tackle, this talk suggests an approach for addressing this problem in context of model-driven engineering where incorrect or incomplete changes are detectable in form of the inconsistencies they cause. Understanding the impact of a model changes is thus analogous to the detection and repairing of inconsistencies introduced during these changes.
Magne Jørgensen

Things aren’t always what they seem: Three examples of seemingly proper statistical analyses leading to unsubstantiated software engineering claims

Abstract

Statistical analyses of field data are common in empirical software engineering. Unfortunately, it may be easy to misinterpret field data, when not sufficiently aware of assumptions and limitations of the statistical methods. My keynote illustrates this problem through a critical examination of the statistical analyses of three software engineering claims: i) Larger projects have on average larger percentage cost overrun than smaller ones, ii) There is typically an economy-of-scale in software development, and iii) There is a strong, almost universal, tendency towards over-optimism in the estimation of software development costs. All three claims are seemingly strongly supported by published analyses of software engineering field data. I this keynote I demonstrate how violations of essential analysis assumptions, in particular related to measurement error in the independent variables of regression models and non-random or non-representative sampling, are likely to have affected the analyses. In fact, there are good reasons to believe that the first two claims are unsubstantiated and that the third claim is strongly exaggerated. Without an increased awareness of the limitations and assumptions of statistical analyses, the software engineering community will continue to be in risk of presenting statistical artifacts as underlying software engineering relationships.
Rich Goldman
Vice President, Corporate Marketing & Strategic Alliances, Synopsys, Inc.
Chief Executive Officer, Synopsys Armenia

Tech and Space, A Symbiotic Relationship

Abstract
This keynote will examine the close linkage between the development of the semiconductor and space industries from the ‘50s to the present. He will explore how the past achievements of both industries have paved the way for astounding new technology and quality advances that will change the way we inhabit our own world and travel beyond it.
**Fadi J. Kurdahi**
Center for Embedded Computer Systems
University of California, Irvine, CA USA

Exploiting Error-Awareness in System Design

**Abstract**

This talk addresses this notion of error-awareness across multiple abstraction layers — application, architectural platform, and technology — for next generation SoCs. The intent is to allow exploration and evaluation of a large, previously invisible design space exhibiting a wide range of power, performance, and cost attributes. To achieve this one must synergistically bring together expertise at each abstraction layer: in communication/multimedia applications, SoC architectural platforms, and advanced circuits/technology, in order to allow effective co-design across these abstraction layers. As an example, one may investigate methods to achieve acceptable QoS at different abstraction levels as a result of intentionally allowing errors to occur inside the hardware with the aim of trading that off for lower power, higher performance and/ or lower cost. Such approaches must be validated and tested in real applications. An ideal context for the convergence of such applications are handheld multimedia communication devices in which a WCDMA modem and an H.264 encoder must co-exist, potentially with other applications such as imaging. These applications have a wide scope, execute in highly dynamic environments and present interesting opportunities for tradeoff analysis and optimization. We also demonstrate how error awareness can be exploited at the architectural platform layer through the implementation of error tolerant caches that can operate at very low supply voltage.
Multicore Platform Design: Tackling a Grand Challenge in Embedded Computing

Abstract

Due to power and performance reasons, multicore (or MPSoC) architectures are getting widespread in virtually all domains of computing. Their HW/SW design constraints are particularly tight in wireless communication devices. The amount of mobile data traffic is expected to grow by 1000x within the next decade, resulting in very high performance requirements. At the same time, especially in battery driven devices, maximum energy efficiency is a must.

Moreover, the problem of how to efficiently implement software on embedded parallel processor architectures is largely unsolved today. This presentation covers several novel system-level design technologies, conceived to help in efficient HW/SW design for multi-billion transistor embedded platforms, with emphasis on the special demands of wireless applications.

The first part will provide an introduction to automated design of application specific processors (ASIPs). Next, we will discuss some recent advances in virtual prototyping and simulation of complex multicore architectures and entire devices. Furthermore, we will sketch the MAPS compiler approach for mapping embedded application software onto heterogeneous parallel target platforms. Finally, we provide an outlook on further key research issues in embedded systems design to support the future “mobile society”.

Rainer Leupers
RWTH Aachen University - Germany
Program

Wednesday, 5 September 2012

08:30 – 09:30 Registration

09:30 – 10:00 Opening
Location: Ballroom

10:00 – 11:00 Keynote Speech – 1 (SEAA – 1)
Location: Ballroom

• Model-Driven Engineering and the Impact of a Change
  Alexander Egyed

11:00 – 11:30 Coffee Break

11:30 – 13:00 Sessions

ESE — 1: Model-based development
Location: Deniz Kızı 3
Chair: Antonio Cicchetti

• DiplodocusDF, a Domain-Specific Modelling Language for Software Defined Radio Applications
  Jair Gonzalez-Pina, Rabea Ameur-Boulifa and Renaud Pacalet

• A MDD Approach for RTOS Integration on Valid Real-Time Design Model
  Rania Mzid, Chokri Mraidha, Jean-Philippe Babau and Mohamed Abid

• Multi-View Power Modeling Based on UML MARTE and SysML
  Carlos Gomez, Julien Deantoni and Frédéric Mallet
SEAA Sessions

MOCS — 1: Product Lines

Location: Gerence 1
Chair: Kung-Kiu Lau

• An Aspect-based Feature Model for Architecting Component Product Lines
  Leonardo Tizzei, Cecilia Rubira, Jaejoon Lee

• TIRT: A Traceability Information Retrieval Tool for Software Product Lines Projects
  Wyliams Barbosa Santos, Eduardo Santana de Almeida, and Silvio Romero de L. Meira

• CodeScoping: A Source Code Based Tool to Software Product Lines Scoping
  Thiago Fernandes Lins de Medeiros, Eduardo Santana de Almeida, and Silvio Romero de Lemos Meira

• A Lightweight Approach for Product Line Scoping
  Markus Nöbauer, Norbert Seyff, Iris Groher, and Deepak Dhungana

SPPI — 1: Agile and Lean Processes

Location: Deniz Kızı 2
Chair: Rudolf Ramler

• Adapting the Lean Enterprise Self-Assessment Tool for the Software Development Domain
  Teemu Karvonen, Pilar Rodriguez, Pasi Kuvaja, Kiri Mikkonen, and Markku Oivo

• Investigating Daily Team Meetings in Agile Software Projects
  Viktoria Gulliksen Stray, Nils Brede Moe, and Aytübe Aurum

• Organizational Values and Agile Methods Deployment
  Stavros Stavru

13:00 – 14:00 Lunch Break

14:00 – 15:00 Keynote Speech — 2 (DSD — 1)

Location: Ballroom

• Exploiting Error-Awareness in System Design
  Fadi J. Kurdahi
15:00 – 16:00 Sessions

**ESE – 2: Formal Methods**

*Location:* Deniz Kızı 3  
*Chair:* Tomas Bures

- A Property-Based Proof System for Contract-Based Design  
  Alessandro Cimatti and Stefano Tonetta

- Max-Plus Algebraic Throughput Analysis of Synchronous Dataflow Graphs  
  Robert de Groote, Jan Kuper, Hajo Broersma, and Gerard J.M. Smit

**MOCS – 2: Embedded Systems**

*Location:* Gerence 1  
*Chair:* Mauro Caporuscio

- Ensuring Component Application Consistency on Small Devices: A Repository-Based Approach  
  Premek Brada and Kamil Ježek

- Towards a Model-Based Approach for Allocating Tasks to Multicore Processors  
  Juraj Feljan, Jan Carlson, and Tiberiu Seceleanu

**SPPI – 2: Process Improvement and Quality**

*Location:* Deniz Kızı 2  
*Chair:* Fritz Stallinger

- Random Test Case Generation and Manual Unit Testing: Substitute or Complement in Retrofitting Tests for Legacy Code?  
  Rudolf Ramler, Dietmar Winkler, and Martina Schmidt

- A Case Study on Measuring Process Quality: Lessons Learned  
  Ahmet Dikici, Oktay Turetken, and Onur Demirors

- From Assumptions to Context-Specific Knowledge in the Area of Combined Static and Dynamic Quality Assurance  
  Frank Elberzhager and Thomas Bauer

- Micro Pattern Fault Proneness  
  Giuseppe Destefanis, Roberto Tonelli, Ewan Tempero, Giulio Concas, and Michele Marchesi

16:00 – 16:30 Coffee Break
16:30 – 17:30 Sessions

**ESE – 3: Certification and Tool Support**

**Location:** Deniz Kızı 3  
**Chair:** TBD

- **A Framework for the Development of Parallel and Distributed Real-Time Embedded Systems**  
  Ricardo Garibay-Martinez, Luis Lino Ferreira, and Luis Miguel Pinho

- **Structuring Modular Safety Software Certification by Using Common Criteria Concepts**  
  Christopher Preschern and Kurt Dietrich

- **Database Proxy Tool Support in an AUTOSAR Development Environment**  
  Andreas Hjertström, Dag Nyström, and Mikael Sjödin

**MOCS – 3: Extra-functional Properties**

**Location:** Gerence 1  
**Chair:** Premek Brada

- **Reliability Prediction for Service Component Architectures with the SCA-ASM Component Model**  
  Elvinia Riccobene, Pasqualina Potena, and Patrizia Scandurra

- **Path Coverage Criteria for Palladio Performance Models**  
  Henning Groenda

- **Using Virtual Machine Security to Reinforce Components Constraints**  
  Aurélio A.M. Matsui, Straus Michalsky, and Marco Aurélio Gerosa

**SPPI – 3: Process and Product Modeling**

**Location:** Deniz Kızı 2  
**Chair:** Aybüke Aurum

- **From Software to Software System Products: An Add-on Process Reference Model for Enhancing ISO/IEC 12207 with Product Management and System-Level Reuse**  
  Fritz Stallinger, Robert Neumann

- **Towards a Metamodel for integrating Multiple Models for Process Improvement**  
  Edgar L. Banhesse, Clenio F. Salviano, and Mario Jino

- **The Barriers to Traceability and their Potential Solutions: Towards a Reference Framework**  
  Gilbert Regan, Fergal McCaffery, Kevin McDaid, and Derek Flood

- **A Practice for Recording Problem and Solution Domain Requirements in VLSRE**  
  Markus Kelanti, Jari Lehto, Sanja Aaramaa, and Pasi Kuova
Thursday, 6 September 2012

08:30 – 09:00 Registration

09:00 – 10:00 Keynote Speech – 3 (DSD – 2)
Location: Ballroom

• Multicore Platform Design: Tackling a Grand Challenge in Embedded Computing
  Rainer Leupers

10:00 – 10:30 Coffee Break

10:30 – 12:30 Sessions

ESE – 4: Analysis and Synthesis
Location: Deniz Kizi 3
Chair: TBD

• Analyzing Long-Running Controller Applications for Specification Violations Based on Deterministic Replay
  Roland Schatz and Herbert Prahofer

• Varying Topology of Component-Based System Architectures Using Metaheuristic Optimization
  Ramin Etemaadi and Michel R.V. Chaudron

• Towards Automatic Synthesis of Hardware-Specific Code in Component-Based Embedded Systems
  Luka Lednicki, Ivica Crnkovic, and Mario Žagar

• A Bridge from System to Software Development for Safety-Critical Automotive Embedded Systems
  Roland Mader, Gerhard Griebig, Eric Armengaud, Andrea Leitner, Christian Kreiner, Quentin Bourrouilh, Christian Steger, and Reinhold Weiß

• Real-Time Component Integration Using Runnable Virtual Nodes
  Rafia Inam, Jukka Mäki-Turja, Mikael Sjödin, and Jiří Kuncar

MOCS – 4: Modeling Components
Location: Gerence 1
Chair: TBD

• Toward Model-Based Trade-off Analysis of Non-Functional Requirements
  Mehrdad Saadatmand, Antonio Cicchetti, and Mikael Sjödin

• An MDE Approach for Runtime Monitoring and Adapting Component-Based Systems: Application to WIMP User Interface Architectures
  Javier Criado, Luis Iríbarne, Nicolás Padilla, Javier Troya, and Antonio Vallecillo
• X-MAN: An MDE Tool for Component-Based System Development
  
  *Kung-Kiu Lau and Cuong M. Tran*

• A Model-Driven Engineering Framework for Fault Tolerance in Dependable Embedded Systems Design
  
  *Adel Ziani, Brahim Hamid, and Jean-Michel Bruel*

• Automatic Adaptation of Transformations Based on Type Graph with Multiplicity
  
  *Quyet-Thang Pham and Antoine Beugnard*

**SM — 1: Software Management**

*Location: Deniz Kızı 2*

*Chair: TBD*

• An Investigation of Software Effort Phase Distribution Using Compositional Data Analysis
  
  *Panagiota Chatzipetrou, Efi Papatheocharous, Lefteris Angelis, and Andreas S. Andreou*

• Developers Motivation in Agile Teams
  
  *Claudia de O. Melo, Célio Santana, and Fabio Kon*

• A Fuzzy Multi Criteria Decision Making Approach to Software Life Cycle Model Selection
  
  *Mümin Hiçdurmaz*

• Climbing the “Stairway to Heaven”—A Multiple-Case Study Exploring Barriers in the Transition from Agile Development towards Continuous Deployment of Software
  
  *Helena Holmström Olsson, Hiva Alahyari, and Jan Bosch*

**12:30 – 13:30 Lunch Break**

**13:30 – 14:30 Keynote Speech — 4 (DSD — 3)**

*Location: Ballroom*

• Tech and Space, A Symbiotic Relationship
  
  *Rich Goldman*

**14:30 – 15:30 Sessions**

**Cloud—1: Cloud Technology**

*Location: Deniz Kızı 3*

*Chair: Keijo Heljanko*

• Feedback Control Algorithms to Deploy and Scale Multiple Web Applications per Virtual Machine
  
  *Adnan Ashraf, Benjamin Byholm, Joonas Lehtinen, and Ivan Porres*

• Towards Mobile Multimedia Mashup Architecture
  
  *Mikko Hartikainen, Arto Salminen, and Jarno Kallio*
MOCS — 5: Frameworks and Architecture

Location: Gerence 1
Chair: George Kakarontas

- Testing a Component-Based Application for Road Traffic Crossroad Control Using the SimCo Simulation Framework
  Tomáš Potužák, Richard Lipka, Premek Brada, and Pavel Herout

- ORCA: Architecture for Business Tier Components Driven by Dynamic Adaptation and Based on Call Level Interfaces
  Óscar Mortágua Pereira, Rui Luís Aguiar, and Maribel Yasmina Santos

15:30 – 16:00 Coffee Break

16:00 – 17:00 Sessions

Cloud—2: Cloud Software

Location: Deniz Kızı 3
Chair: Keijo Heljanko

- A Model for Global Software Development with Cloud Platforms
  Luisanna Cocco, Katuscia Mannaro, and Giulio Concas

- Differentiation in the Cloud: Methodology for Integrating Customer Values in Experience Design
  Andrey Sirotkin, Kaisa Keskela-Huotari, Kaarina Karppinen, Javier Del Ser, and Bronan McCabe

MOCS — 6: Finding and Building Components

Location: Gerence 1
Chair: Tomas Bures

- Extracting Components from Open Source: The Component Adaptation Environment (COPE) Approach
  George Kakarontzas, Ioannis Stamelos, Stefanos Skalistis and Athanasios Naskos

- Federated Search for Open Source Software Reuse
  Fotios Kokkoras, Konstantinos Ntonas, Apostolos Kritikos, George Kakarontzas, and Ioannis Stamelo

- Application and UI Composition Using a Component-Based Description and Annotations
  Christian Brel, Philippe Renevier-Gonin, Anne-Marie Pinna-Déry, and Michel Riveill

Special Session: MeSVAM — Measurement as a Strategy for Software Value Management

Location: Deniz Kızı 2
Chair: Cigdem Gencel

- Managing Software Quality Requirements
  Laura Phillips, Aybuke Aurum, and Richard Berntsson Svensson
• Software Measurement in Software Engineering Education: A Delphi Study to Develop a List of Teaching Topics and Related Levels of Learning
  Mónica Villavicencio and Alain Abran

• Value-Based Coverage Measurement in Requirements-Based Testing: Lessons Learned from an Approach Implemented in the TOSCA Testsuite
  Rudolf Ramler, Theodorich Kopetzky, Wolfgang Platz
Friday, 7 September 2012

08:30 – 09:00 Registration

09:00 – 10:00 Keynote Speech – 5 (SEAA-2)
Location: Ballroom

• Things aren’t always what they seem: Three examples of seemingly proper statistical analyses leading to unsubstantiated software engineering claims
  Magne Jørgensen

10:00 – 10:30 Coffee Break

10:30 – 12:30 Sessions

Tutorial
Location: Deniz Kızı 3

• Using Multiple Models for Process Improvement
  Clenio Salviano

MOCS – 7: Modeling Services and Components
Location: Gerence 1
Chair: Brahim Hamid

• Engineering Emergent Semantics into Pervasive Resource Discovery
  Mauro Caporuscio

• Low-Level Profiling and MARTE-Compatible Modeling of Software Components for Real-Time Systems
  Konstantinos Triantafyllidis, Egor Bondarev, and Peter H. De With

• LogOS: An Automatic Logging Framework for Service-Oriented Architectures
  Stéphane Frénot and Julien Ponge

• FOAM: A Lightweight Method for Verification of Use-Cases
  Viliam Simko, Petr Hnetynka, Tomas Bures, and Frantisek Plasil

• A Model-Driven Dependability Analysis Method for Component-based Architectures
  Barbara Gallina, Muhammad Atif Javed, Faiz Ul Muram, and Sasikumar Punnekkat
SEAA Sessions

**SM — 2: Software Management**

**Location:** Deniz Kızı 2  
**Chair:** TBD

- Towards the Understanding and Classification of the Personality Traits of Software Development Practitioners: Situational Context Cards Approach  
  *Murat Yılmaz and Rory V. O’Connor*

- Guiding Testing Activities by Predicting Defect-Prone Parts Using Product and Inspection Metrics  
  *Frank Elberzhager, Stephan Kremer, Jürgen Münch, and Danilo Assmann*

- An Analysis of Accuracy and Learning in Software Project Estimating  
  *A.H. Zapata and M.R.V. Chaudron*

- Pocket Estimator—a Commercial Solution to Provide Free Parametric Software Estimation Combining an Expert and a Learning Algorithm  
  *Florian Schnitzhofer and Peter Schnitzhofer*

- Estimating the Return on Investment of Defect Taxonomy Supported System Testing in Industrial Projects  
  *Michael Felderer and Armin Beer*

**12:30 — 13:30 Lunch Break**

**13:30 — 15:00 Sessions**

**MOCS — 8: Special Sessions Papers: Cyber-Physical Systems and Distributed Architectures**

**Location:** Gerence 1  
**Chair:** Horst F. Wedde and Karl-Erwin Grosspietsch

- DEZENT — A Cyber-Physical Approach for Providing Affordable Renewable Electric Energy in the Near Future  
  *Horst F. Wedde (Invited)*

- Applying the Organic Robot Control Architecture ORCA to Cyber-Physical Systems  
  *Raphael Maas, Erik Maehle, Karl-Erwin Großpietsch (Invited)*

- Bee-Inspired Road Traffic Control as an Example of Swarm Intelligence in Cyber-Physical Systems  
  *Sebastian Senge and Horst F. Wedde (Invited)*

**SPPI — 4: Practical Experiences and New Ideas for Process Improvement**

**Location:** Deniz Kızı 2  
**Chair:** Frank Elberzhager

  *Nauman Bin Ali and Kai Petersen*
• Fostering Cross-site Coordination through Awareness: An Investigation of State-of-the-Practice through a Focus Group Study
  Darja Šmite and Torgeir Dingsøyr

• Low Degree of Separation Does Not Guarantee Easy Coordination
  Zane Galvina, Darja Šmite

15:00 – 15:30 Coffee Break

15:15 – 17:30 Sessions

**WiP: SEAA/DSD Work in Progress**

*Location:* Deniz Kızı 3

*Chair:* K. Klöckner, K.E. Grosspietsch

• Cost-Efficient Resource Allocation for Multi-tier Web Applications in a Cloud Environment
  Adnan Ashraf

• Goal-Business Process Integration through Choreography within Enterprise Architecture
  Cahit Gungor

• Algorithmic vs Architectural Optimizations in a C-Based PLC to FPGA Translation Environment
  Christoforos Economakos and George Economakos

• Measuring Software Engineer Motivation in Globally Distributed Projects
  Liva Šteinberga

• QoS-enabled Middleware for Smart Grids
  Abdel Rahman, Alkhavaja, Luis Lino Ferreira, Michele Albano, and Ricardo Garibay

• A Proposal for Multidisciplinary Software for People with Autism
  Eraldo Guerra and Felipe Furtado

• High Breakdown Voltage and Switching Speed IGBT Design
  A. Belous, I. Lovshenko, V. Nelayev, A. Turtsevich, and I. Shelibak

• Design Methodology for Implementing Multiplexer Based Ternary Logic Circuits Using Carbon Nanotube Field Effekt Transistor (CNFET)
  Chetan Vudadha, P. Sai Phaneendra, V. Sreehari, and M.B. Srinivas

• A Haskell-Based Programming Paradigm for Coarse-Grained Reconfigurable Arrays
  Anja Niedermeier, Jan Kuper, and Gerard Smit

• Visual Exploration of Changing FPGA Architectures in the VTR Project
  Konstantin Nasartschuk, Kenneth B. Kent, and Rainer Herpers
• Design Synchronization after Partial Dynamic Reconfiguration of Fault Tolerant System
  *Lukas Miculka and Zdenek Kotasek*

• Analysis Approach for Safety Critical Hardware using Neural Networks
  *M. Schmedes, A. Th. Schwarzbacher, and B. Hoppe*

• Error-Resilient BDDs: A Preliminary Study
  *Lorenzo Lago, Anna Bernasconi, and Valentina Ciriani*

17:30 – 18:00 Closing

*Location:* Ballroom
<table>
<thead>
<tr>
<th>Time</th>
<th>Kizi 2</th>
<th>Ballroom</th>
<th>Gerence 2</th>
<th>Gerence 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>08:00-09:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>09:00-09:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>09:30-10:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10:00-10:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10:30-11:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11:00-11:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11:30-12:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12:00-12:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12:30-13:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13:00-13:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13:30-14:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14:00-14:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14:30-15:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:00-15:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:30-16:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16:00-16:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16:30-17:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17:00-17:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17:30-18:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18:00-18:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18:30-19:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>19:00-19:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>19:30-20:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20:00-20:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20:30-21:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21:00-21:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21:30-22:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22:00-22:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22:30-23:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:00-23:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:30-00:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Friday, September 07, 2012**

<table>
<thead>
<tr>
<th>Time</th>
<th>Deniz Kizi 3</th>
<th>Gerence 1</th>
<th>Deniz Kizi 2</th>
<th>Ballroom</th>
<th>Gerence 2</th>
<th>Gerence 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>08:00-09:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>09:00-09:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>09:30-10:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10:00-10:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11:00-11:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11:30-12:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12:00-12:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12:30-13:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13:00-13:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13:30-14:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14:00-14:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14:30-15:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:00-15:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:30-16:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16:00-16:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16:30-17:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17:00-17:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17:30-18:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18:00-18:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18:30-19:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>19:00-19:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>19:30-20:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20:00-20:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20:30-21:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21:00-21:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21:30-22:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22:00-22:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22:30-23:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:00-23:30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:30-00:00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Conference Dinner**
Things to see in Çeşme

Fortress of Çeşme
- Çeşme Museum
- Ayios Haralambos Church
- Fountains
- Traditional Çeşme Houses
- Çeşme Beaches
  - İlica
  - Boyalık Bay
  - Ayayorgi
  - Dalyan
- Alaçatı Windsurf & Kitesurf

Travel

Those arriving at İzmir Adnan Menderes Airport may take service busses to Çeşme - the journey takes about 45 minutes.

Regular minibus services depart from Çeşme centre to beaches such as Altınkum Dalyan, Alaçatı, Ovacık İlica, Reisdere.
Wednesday, 5 September 2012

8:30 – 9:30 Registration

9:30 – 10:00 Opening

Location: Ballroom

10:00 – 11:00 Keynote Speech — 1 (SEAA — 1)

Location: Ballroom

• Model-Driven Engineering and the Impact of a Change
  Alexander Egyed

11:00 – 11:30 Coffee Break

11:30 – 13:00 Sessions

FTDSD— 1: Fault Tolerance in Digital System Design

Location: Ballroom

Chair: Z. Kotasek

• Impact of duty factor, stress stimuli, and gate drive strength on gate delay degradation with an atomistic trap-based BTI model
  [Best Paper Candidate]
  Halil Kukner, Pieter Weckx, Praveen Raghavan, Ben Kaczer, Francky Catthoor, Liesbet Van der Perre, Rudy Lauwereins, and Guido Groeseneken
• Architecture and Design Analysis of a Digital Single-Event Transient/Upset Measurement Chip  
   [Best Paper Candidate]  
   Varadan Savulimedu Veeravalli, Ulrich Schmid, Andreas Steininger, and Thomas Polzer

• Accurate Estimation of Leakage Power Variability in Sub-Micrometer CMOS Circuits  
   [Best Paper Candidate]  
   Omid Assare, Mahmoud Momtazpour, and Maziar Goudarzi

MORPS—1: Monitoring and Reconfiguration of Parallel Systems  
Location: Gerence 2  
Chair: P. Liljeberg

• ReMORPH -- A Runtime Reconfigurable Architecture  
   Kolin Paul, Chinmaya Dash, and Mansureh Moghaddam

• Designing a High Performance and Reliable Networks-on-Chip using Network Interface Assisted Routing Strategy  
   Khalid Latif, Amir-Mohammad Rahmani, Tiberiu Seceleanu, and Hannu Tenhunen

• A Scalable Monitoring Infrastructure for Self-Organizing Many-Core Architectures  
   David Kramer and Wolfgang Karl

SHES—1: System, Hardware and Embedded Software Design and Automatic Synthesis  
Location: Gerence 3  
Chair: A. Yurdukal

• On the design of configurable modulo $2^n \pm 1$ residue generators  
   Constantinos Efstathiou, Nikos Moschopoulos, Kostas Tsoumanis, and Kiamal Pekmestzi

• Projected Don’t Cares  
   Anna Bernasconi, Valentina Ciriani, Gabriella Trucco, and Tiziano Villa

• SUT-RNS Residue-to-Binary Converters Design  
   Evangelos Vassalos, Dimitris Bakalis, and Haridimos Vergos

13:00 – 14:00 Lunch Break

14:00 – 15:00 Keynote Speech — 2 (DSD – 1)  
Location: Ballroom

• Exploiting Error-Awareness in System Design  
   Fadi J. Kurdahi
15:00 – 16:00 Sessions

**FTDSD – 2: Fault Tolerance in Digital System Design**

*Location:* Ballroom

*Chair:* H. Kubatova

- Automated Generation of Built-in Self-Repair Architectures for Random Logic SoC Cores
  *Roland Dobai, Marcel Balaz, and Maria Fischerova*

- Miscellaneous Types of Partial Duplication Modifications for Availability Improvements
  *Jaroslav Borecký, Martin Kohlík, and Hana Kubátová*

- Reliability of Task Execution during Safe Software Processing
  *Peter Raab, Stanislav Racek, Juergen Mottok, and Stefan Krämer*

**ET – 1: Important Issues Introduced by Emerging Technologies**

*Location:* Gerence 2

*Chair:* D. Quaglia

- Power Optimization Opportunities for a Reconfigurable Arithmetic Component in the Deep Submicron Domain
  *Dimitris Bekiaris and George Economakos*

- OWQS: One-Way Quantum Computation Simulator
  *Eesa Nikahd, Mahboobeh Houshmand, Morteza Saheb Zamani, and Mehdi Sedighi*

**EPDSD – 1: European Projects in DSD**

*Location:* Gerence 3

*Chair:* L. Jozwiak

- The ACROSS MPSoC — A New Generation of Multi-Core Processors designed for Safety-Critical Embedded Systems
  *Christian El Salloum, Martin Elshuber, Oliver Höffberger, Haris Isakovic, and Armin Wasicek*

- From Scilab To High Performance Embedded Multicore Systems — The ALMA Approach
  *Juergen Becker, Timo Stripf, Oliver Oey, Michael Huebner, Steven Derrien, Daniel Menard, Olivier Sentieys, Gerard Rauwerda, Kim Sunesen, Nikolaos Kavvadias, Kostas Masselos, George Goulas, Panayiotis Alefragis, Nikolaos S. Voros, Dimitrios Kritharidis, Nikolaos Mitas, and Diana Goehringer*

16:00 – 16:30 Coffee Break
16:00 – 16:30 *Poster Session — 1*

**Location:** Ballroom

- FPGA based Real-Time Tracking Approach with Validation of Precision and Performance
  *Alexander Bochem, Kenneth Kent, and Rainer Herpers*

- Analyzing Bus Load Data Using an FPGA and a Microcontroller
  *Marcel Dombrowski, Kenneth B. Kent, Yves Losier, Adam Wilson, and Rainer Herpers*

- On the Development of a Runtime Reconfigurable Multicore System-on-Chip
  *Andrea Cazzaniga, Gianluca Durelli, Christian Pilato, Donatella Sciuto, and Marco Domenico Santambrogio*

- Resilient Adaptive Algebraic Architecture for Parallel Detection and Correction of Soft-Errors
  *Fabio Itturriet, Ronaldo Ferreira, Gustavo Girao, Gabriel Nazar, Alvaro Moreira, and Luigi Carro*

- Improving the Soft Error Resilience of the Register Files Using SRAM Bitcells with Built-in Comparators
  *Mehmet Kayaalp, Fahrettin Koc, and Oguz Ergin*

- Vulnerability Analysis For Custom Instructions
  *Ali Azarpeyvand, Mostafa Ersali Salehi Nasab, and Seid Mehdi Fakhraie*

- A Three-Dimensional Integrated Accelerator
  *Farhad Mehdipour, Krishna C. Nunna, Koji Inoue, and Kazuaki J. Murakami*

- Algorithm Parallelism Estimation for Constraining Instruction-Set Synthesis for VLIW Processors
  *Roel Jordans, Rosilde Corvino, and Lech Jozwiak*

16:30 – 18:00 *Sessions*

**AHSA — 1: Architectures and Hardware for Security Applications**

**Location:** Ballroom

**Chair:** P. Kitsos

- An Easy-to-Design PUF based on a single oscillator: the Loop PUF
  *Zouha Cherif, Jean Luc Danger, Sylvain Guilley, and Lilian Bossuet*

- No Principal Too Small: Memory Access Control for Fine-Grained Protection Domains
  *Eugen Leontie, Gedare Bloom, Bhagirath Narahari, and Rahul Simha*

- Hardware Strengthening a Distributed Logging Scheme
  *Jo Vliegen, Karel Wouters, Christian Grahn, and Tobias Pulls*

- Trojan Immune Circuits Using Duality
  *Yousra Alkabani*
MORPS — 2: Monitoring and Reconfiguration of Parallel Systems

Location: Gerence 2
Chair: E. Nigussie

- Semi-distributed control for FPGA-based reconfigurable systems
  Chiraz Trabelsi, Samy Meftali, and Jean-Luc Dekeyser

- FPGA-Based Neural Network for Nonuniformity Correction on Infrared Focal Plane Arrays
  Nicolas Celedon, Rodolfo Redlich, and Miguel Figueroa

- MAFA: Adaptive Fault-Tolerant Routing Algorithm for Networks-on-Chip
  Masoumeh Ebrahimi, Masoud Daneshtalab, Juha Plosila, and Hannu Tenhunen

- Power and Thermal Analysis of Stacked Mesh 3D NoC Using AdaptiveXYZ Routing Algorithm
  Amir-Mohammad Rahmani, Kameswar Rao Vaddina, Pasi Liljeberg, Juha Plosila, and Hannu Tenhunen

EPDSD — 2: European Projects in DSD

Location: Gerence 3
Chair: F. Leporati

- ASAM: Automatic Architecture Synthesis and Application Mapping
  Lech Jozwiak, Menno Lindwer, Rosilde Corvino, Paolo Meloni, Laura Micconi, Jan Madsen, Erkan Diken, Deepak Gangadharan, Roel Jordans, Sebastiano Pomata, Paul Pop, Giuseppe Tuveri, and Luigi Raffo

- Controlling Hardware Synthesis with Aspects
  João M.P. Cardoso, Tiago Carvalho, José G.F. Coutinho, Pedro Diniz, Zlatko Petrov, and Wayne Luk

- FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration
  Dionisios Pnevmatikatos, Tobias Becker, Andreas Brokalakis, Karel Bruneel, Georgi Gaydadjiev, Wayne Luk, Kyprianos Papadimitriou, Ioannis Papaefstathiou, Oliver Pell, Christian Pilato, Mathieu Robart, Marco Santambrogio, Donatella Sciuto, Dirk Stroobandt, and Tim Todman
Thursday, 6 September 2012

8:30 – 9:00 Registration

9:00 – 10:00 Keynote Speech – 3 (DSD – 2)
Location: Ballroom

• Multicore Platform Design: Tackling a Grand Challenge in Embedded Computing
  Rainer Leupers

10:00 – 10:30 Coffee Break

10:30 – 12:30 Sessions

FTDSD – 3: Fault Tolerance in Digital System Design
Location: Ballroom
Chair: R. Dobai

• Energy-aware Fault-tolerant Network-on-chips for Addressing Multiple Traffic Classes
  Syed Mohammad Asad Hassan Jafri, Liang Guang, Ahmed Hemani, Juha Plosila, Kolin Paul, and Hannu Tenhunen

• Dependability Analysis of Fault Tolerant Systems Based on Partial Dynamic Reconfiguration Implemented into FPGA
  Jan Kastil, Martin Straka, Lukas Miculka, and Zdenek Kotasek

• Activity Migration in M-of-N-Systems by means of Load-Balancing
  Markus Ulbricht, Heinrich Theodor Vierhaus, and Tobias Koal

• Protecting an Asynchronous NoC against Transient Channel Faults
  Syed Rameez Naqvi, Varadan Savulimedu Veeravalli, and Andreas Steininger

• On Distribution and Impact of Fault Effects at Real-Time Kernel and Application Levels
  Josef Strnadel and Frantisek Slimarik

• Exploiting Bus Level and Bit Level Inactivity for Preventing Wire Degradation due To Electromigration
  Mehmet Kayaalp, Fahrettin Koc, and Oguz Ergin

SoC&NoC – 1: Systems and Networks on Chip
Location: Gerence 2
Chair: O. Ozturk

• A Heuristic Energy-Aware Approach for Hard Real-Time Systems on Multi-Core Platforms
  [Best Paper Candidate]
  Da He and Wolfgang Mueller
DSD Sessions

• ONC3: All-Optical NoC based on Cube-Connected Cycles with Quasi-DOR Algorithm
  [Best Paper Candidate]
  Meisam Abdollahi, Mohammad Khavari Tavana, Somayyeh Koohi, and Shaahin Hessabi

• Architecture Support and Comparison of Three Memory Consistency Models in NoC based Systems
  Abdul Naeem, Axel Jantsch, and Zhonghai Lu

• A Simple On-chip Optical Interconnection for Improving Performance of Coherency Traffic in CMPs
  Sandro Bartolini and Paolo Grani

• High Speed Dynamic Partial Reconfiguration for Real Time Multimedia Signal Processing
  S. Bhandari, S. Subbaraman, S. Pujari, F. Cancare, F. Bruschi, M.D. Santambrogio, and P.R. Grassi

EPDSD – 3: European Projects in DSD

Location: Gerence 3
Chair: E. Villar

• The Seat Adaptation System of REFLECT Project: Implementation of a Byocibernetic Loop in an Automotive Environment
  Gian Mario Bertolotti, Andrea Cristiani, Remo Lombardi, and Nikola Serbedzija

• The DeSyRe project: on-Demand System Reliability
  Ioannis Sourdis, Christos Strydis, Christos-Savvas Bouganis, Babak Falsafi, Georgi N. Gaydadjiev, Alirad Malek, Riccardo Mariani, Dionisios N. Pnevmatikatos, Dhiraj K. Pradhan, Gerard Rauwerda, Kim Sunesen, and Stavros Tzilis

• FASTCUDA: Open Source FPGA Accelerator & Hardware-Software Codesign Toolset for CUDA Kernels
  Iakovos Mavroidis, Ioannis Mavroidis, Ioannis Papaeftathiou, Luciano Lavagno, Mihai Lazarescu, Eduardo de la Torre, and Florian Schäfer

• COMPLEX - COdesign and power Management in PLaform-based design space Exploration
  Kim Grüttrner, Philipp A. Hartmann, Kai Hyllo, Sven Rosinger, Wolfgang Nebel, Fernando Herrera, Eugenio Villar, Carlo Brandolese, William Fornaciari, Gianluca Palermo, Chantal Ykman-Couvreur, Davide Quaglia, Francisco Ferrera, and Raúl Valencia

12:30 – 13:30 Lunch Break

13:30 – 14:30 Keynote Speech – 4 (DSD – 3)
Location: Ballroom

• Tech and Space, A Symbiotic Relationship
  Rich Goldman
DSD Sessions

14:30 – 15:30 Sessions

**DTDS – 1: Dependability and Testing of Digital Systems**

*Location:* Ballroom

*Chair:* H. Kubátová

- Using Genetic Algorithm to Identify Soft-Error Derating Blocks of an Application Program
  *Bahman Arasteh, Amir Masoud Rahmani, Ali Mansoor, and Seyed Ghassem Miremadi*

- The Influence of Implementation Technology on Dependability Parameters
  *Jan Schmidt, Petr Fiser, and Jiří Balcárek*

**ET – 2: Important Issues Introduced by Emerging Technologies**

*Location:* Gerence 2

*Chair:* F. Mehdipour

- TSV-Virtualization for Multi-Protocol-Interconnect in 3D-ICs
  *Felix Miller, Thomas Wild, and Andreas Herkersdorf*

- A Methodology for Early Exploration of TSV Placement Topologies in 3D Stacked ICs
  *Radhika Jagtap, Sumeet S. Kumar, and Rene Van Leuken*

**SHES – 2: System, Hardware and Embedded Software Design and Automatic Synthesis**

*Location:* Gerence 3

*Chair:* I. Sourdis

- Multi-Device Driver Synthesis Flow for Heterogeneous Hierarchical Systems
  *Alexandre Chagoya-Garzon, Frédéric Pétrot, and Frederic Rousseau*

- A Verifiable High Level Data Path Synthesis Framework
  * Görker Alp Malazgirt, Ender Culha, Alper Sen, Faik Baskaya, and Arda Yurdakul*

- Finite State Machine Synthesis Based on Relay-Based algorithm
  *Meng Yang, Jinmei Lai, and Hongying Xu*

15:30 – 16:00 Coffee Break
15:30 – 16:00 Poster Session — 2

Location: Ballroom

- VLSI Reverse Converter for RNS based on the Moduli Set \( \{2^n + 1, 2^n - 1, 2^{2n+1} - 3, 2^{2n} - 2\} \)
  Leonel Sousa and Samuel Antao

- EJOP: an Extensible Java Processor with Reasonable Performance/Flexibility Trade-off
  Samaneh Talebi, Ali Jahanian, and Niloofar Abolghasemi

- A dual-core coprocessor with native 4D Clifford algebra support
  Silvia Franchini, Antonio Gentile, Giorgio Vassallo, Salvatore Vitabile, and Filippo Sorbello

- SystemC model generation for realistic simulation of networked embedded systems
  Mihai Lazarescu, Parinaz Sayyah, Davide Quaglia, and Francesco Stefanni

- How to Prove that a Circuit is Fault-Free?
  Raimund Ubar, Sergei Kostin, and Jaan Raik

- On Modeling and Evaluation of Logic Circuits Under Timing Variations
  Mehdi Dehbashi, Görschwin Fey, Kaushik Roy, and Anand Raghunathan

16:00 – 18:00 Sessions

FDR: Flexible Digital Radio

Location: Ballroom
Chair: D. Noguet

- IEEE 802.11p Receiver Design for Software Defined Radio Platforms
  Carina Schmidt-Knorreck, Daniel Knorreck, and Raymond Knopp

- Analytical Design Space Exploration based on statistically Refined Runtime and Logic Estimation for Software Defined Radios
  Matthias Ihnig, Michael Feilen, and Andreas Herkersdorf

- HDCRAM Proof-of-Concept for Opportunistic Spectrum Access
  Oussama Lazzar, Pierre Leray, and Christophe Moy

- A Flexible Hardware Platform for Mobile Cognitive Radio applications
  Vincent Berg, Dominique Noguet, and Xavier Popon

- Flexible OFDM waveform for PLC/RF in-vehicle communications
  Fabienne Nouvel and Philippe Tanguy
DSD Sessions

DHCPS: Design of Heterogeneous Cyber-Physical Systems

Location: Gerence 2
Chair: D. Quaglia

- Open Problems in Verification and Refinement of Autonomous Robotic Systems
  Davide Bresolin, Luigi Di Guglielmo, Luca Geretti, Riccardo Muradore, Paolo Fiorini, and Tiziano Villa

- Cyber-Physical Systems Design for Electric Vehicles
  Martin Lukasiewycz, Sebastian Steinhorst, Florian Sagstetter, Wanli Chang, Peter Waszecki, Matthias Kauer, and Samarjit Chakraborty

- Simulation-based analysis of cyberphysical systems
  Masahiro Fujita

- Model Checking on Hybrid Automata: Theory and Application to Biological Systems
  Alberto Casagrande and Carla Piazza

EPDSD – 4: European Projects in DSD

Location: Gerence 3
Chair: F. Leporati

- Apple-CORE: Microgrids of SVP Cores — Flexible, General-Purpose, Fine-Grained Hardware Concurrency Management
  Raphael Poss, Mike Lankamp, Chris Jesshope, Michiel W. van Tol, Qiang Yang, and Jian Fu

- HEAP: a Highly Efficient Adaptive multi-Processor framework
  Luciano Lavagno, Mihai Lazarescu, Johan Walters, Bart Kienhuis, Ioannis Papaefstathiou, Andreas Brokalakis, and Florian Schäefer

- System Adaptivity and Fault-tolerance in NoC-based MPSoCs: the MADNESS Project Approach
  Paolo Meloni, Giuseppe Tuveri, Luigi Raffo, Emanuele Cannella, Todor Stefanov, Onur Derin, Leandro Fiorin, and Mariagiovanna Sami
Friday, 7 September 2012

8:30 – 9:00 Registration

9:00 – 10:00 Keynote Speech — 5 (SEAA- 2)
Location: Ballroom
- Things aren’t always what they seem: Three examples of seemingly proper statistical analyses leading to unsubstantiated software engineering claims
  Magne Jørgensen

10:00 – 10:30 Coffee Break

10:00 – 10:30 Poster Session — 3
Location: Ballroom
- Coverage-driven Stimuli Generation
  Shuo Yang, Robert Wille, Daniel Grosse, and Rolf Drechsler
- Convolutional Decoding on Deep-pipelined SIMD Processor with Flexible Parallel Memory
  Jian Wang, Andreas Karlsson, Joar Sohl, and Dake Liu
- Evaluation of the Hardware Performance Space of SHA-3 Candidates Blue Midnight Wish and CubeHash using FPGAs
  Robert Lorentz and Kris Gaj
- Hardware Acceleration of STON Algorithm for Comparing 3-D Structure of Proteins
  Somayeh Kashi and Morteza Sahebzamani
- High Level Modeling and Simulation of a Baseband Processor for the 60 GHz Band
  Ruben Cabral and Helena Sarmento
- A virtual platform for performance estimation of many-core implementations
  Pablo González De Aledo, Javier González-Bayón, and Pablo Sanchez
- Open-People: Open-Power and Energy Optimization Platform and Estimator
  E. Senn, D. Chillet, O. Zendra, C. Belleudy, S. Bilavarn, R. Ben Atitallah, C. Samoyeu, and A. Fritsch
10:30 – 12:30 Sessions

**AHSA — 2: Architectures and Hardware for Security Applications**

**Location:** Ballroom

**Chair:** P. Kitsos

- Differential Scan Attack on AES with X-Tolerant and X-Masked Test Response Compactor
  *Amitabh Das, Baris Ege, Santosh Ghosh, and Ingrid Verbauwhede*

- A Parallel Architecture for Koblitz Curve Scalar Multiplications on FPGA Platforms
  *Sujoy Sinha Roy, Chester Rebeiro, and Debdeep Mukhopadhyay*

- Evaluating Cryptanalytical Strength of Lightweight Cipher PRESENT on Reconfigurable Hardware
  *Jan Pospisil and Martin Novotny*

- A High-Speed Unified Hardware Architecture for the AES and SHA-3 Candidate Gr"ostl
  *Marcin Rogawski and Kris Gaj*

**SoC&NoC — 2: Systems and Networks on Chip**

**Location:** Gerence 2

**Chair:** B. Juurlink

- Minimizing Power Consumption of Spatial Division based Networks-on-Chip Using Multi-Path and Frequency Reduction
  *Sheng Hao Wang, Anup Das, Akash Kumar, and Henk Corporaal*

- Optimal 2D Data Partitioning for DMA Transfers on MPSoCs
  *Selma Saidi, Oded Maler, Pranav Tendulkar, and Thierry Lepley*

- Distance-Constrained Force-Directed Process Mapping for MPSoC Architectures
  *Timo Schönwald, Alexander Viehl, Oliver Bringmann, and Wolfgang Rosenstiel*

- Reducing Instruction Issue Overheads in Application Specific Vector Processors
  *Jaroslav Sykora, Roman Bartosinski, Lukas Kohout, Martin Danek, and Petr Honzik*

**APP — 1: Applications of (Embedded) Digital Systems**

**Location:** Gerence 3

**Chair:** D. Chillet

- Partitioning and Assignment Exploration for Multiple Modes of IEEE 802.11n Modem on Heterogeneous MPSoC Platforms
  *Prashant Agrawal, Kanishk Sugand, Martin Palkovic, Praveen Raghavan, Liesbet Van der Perre, and Francky Catthoor*
• Adaptive Field Strength Scaling - A Power Optimization Technique for Contactless Reader / Smart Card Systems
  Norbert Druml, Manuel Menghin, Christian Steger, Reinhold Weiss, Andreas Genser, Holger Bock, and Josef Haid

• RF-Interconnect Resource Assignment and Placement Algorithms in Application Specific ICs to Improve Performance and Reduce Routing Congestion
  Bahareh Pourshirazi and Ali Jahanian

• High Performance Unified Architecture for Forward and Inverse Quantization in H.264/AVC
  Tiago Dias, Luís Rosário, Nuno Roma, and Leonel Sousa

12:30 – 13:30 Lunch Break

13:30 – 15:00 Sessions

AHSA – 3: Architectures and Hardware for Security Applications
Location: Ballroom
Chair: F. Leporati

• JAAVR: Introducing the Next Generation of Security-enabled RFID Tags
  Erich Wenger, Thomas Baier, and Johannes Feichtner

• FPGA-based Design Approaches of Keccak Hash Function
  George Provelengios, Paris Kitsos, Nicolas Sklavos, and Christos Koulamas

• PROCOMON - An Automatically Generated Predictive Control-Signal Monitor
  Armin Krieg, Johannes Grinschgl, Norbert Druml, Christian Steger, Reinhold Weiss, Holger Bock, and Josef Haid

• CRT RSA Hardware Architecture with Fault and Simple Power Attack Countermeasures
  Apostolos Fournaris and Odysseas Koufopavlou

Location: Gerence 2
Chair: P. Sanchez

• Open-People: Open-Power and Energy Optimization Platform and Estimator
  E. Senn, D. Chillet, O. Zendra, C. Belleudy, S. Bilavarn, R. Ben Atitallah, C. Samoyeau, and A. Fritsch

• An Hardware-In-the-Design Methodology for Wireless Sensor Networks based on Event-Driven Impulse Radio Ultra-Wide Band
  Alberto Bonanno, Alessandro Sanginario, Marco Crepaldi, and Danilo Demarchi

• Energy characterization and classification of embedded operating system services
  Bassem Ouni, Cécile Belleudy, and Eric Senn
**SMVT: System, Hardware and Embedded Software Specification, Modeling, Verification and Test**

**Location:** Gerence 3  
**Chair:** A.M. Molnos

- Enhanced IP-XACT Platform Descriptions for Automatic Generation from UML/MARTE of Fast Performance Models for DSE  
  Fernando Herrera, Héctor Posadas, Eugenio Villar, and Daniel Calvo

- Automated Generation of Embedded Systems Software from timed DEVS Model of Computation Specifications  
  H. Gregor Molter, Johannes Kohlmann, and Sorin A. Huss

- Generation of VHDL code from UML/MARTE sequence diagrams for verification and synthesis  
  Emad Samuel Malki Ebeid, Franco Fummi, and Davide Quaglia

- Extending MARTE to support the specification and the generation of data-intensive applications for Massively Parallel SoC  
  Manel Ammar, Mouna Baklouti, and Mohamed Abid

*15:00 – 15:30 Coffee Break*

**Location:** Ballroom

- Managing a Massively-Parallel Resource-Constrained Computing Architecture  
  Cameron Patterson, Thomas Preston, Francesco Galluppi, and Steve Furber

- Evaluation of a Connectionless NoC for a Real-Time Distributed Shared Memory Many-Core System  
  Jochem H. Rutgers, Marco J.G. Bekooij, and Gerard J.M. Smit

- CoolMap: A Thermal-Aware Mapping Algorithm For Application Specific Networks-on-Chip  
  Mostafa Moazzen, Akram Reza, and Midia Reshadi

- Efficient DPA-Resistance Verification Method with Smaller Number of Power Traces on AES Cryptographic Circuit  
  Hiroki Ito, Mitsuru Shiozaki, Anh-Tuan Hoang, and Takeshi Fujino

- A Distributed Feedback Control Mechanism for Quality-of-Service Maintenance in Wireless Sensor Networks  
  Marcel Steine, Marc Geilen, and Twan Basten
DSD Sessions

15:30 – 17:30 Sessions

**MSDA: Multicore Systems: Design and Applications**

*Location:* Gerence 1

*Chair:* H. Corporaal

- MAMOT: Memory-Aware Mapping Optimization Tool for MPSoC
  Olivera Jovanovic, Iuliana Bacivarov, Peter Marwedel, and Lothar Thiele

- OpenMP-based Synergistic Parallelization and HW Acceleration for On-Chip Shared-Memory Clusters
  Paolo Burgio, Andrea Marongiu, Dominique Heller, Cyrille Chavet, Philippe Coussy, and Luca Benini

- A Game Theoretical Thermal—Aware Run—Time Task Synchronization Method for Multiprocessor Systems—on—Chip
  Yasar Asgarieh, Mohammad Khazzabian, Mehdi Modarressi, and Hamid Sarbazi-Azad

- Composable Virtual Memory for an Embedded SoC
  Cor Meenderinck, Anca Molnos, and Kees Goossens

- Transformation-based Exploration of Data Parallel Architecture for Customizable Hardware: A JPEG Encoder Case Study
  Rosilde Corvino, Erkan Diken, Abdoulaye Gamatie, and Lech Jozwiak

**SHES – 3: System, Hardware and Embedded Software Design and Automatic Synthesis**

*Location:* Deniz Kızı 2

*Chair:* A. Yurdukal

- Efficient Parallel Decimal Multipliers and Squarers using Karatsuba-Ofman’s Algorithm
  Mário Véstias and Horacio Neto

- The Synthesis of Combined Mealy and Moore Machines Structural Model Using Values of Output Variables as Codes of States
  Adam Klimowicz and Valery Salauyou

- RNS Arithmetic Units for Modulo \(2^{n+k}\)
  Pedro Miguens Matutino, Hector Pettenghi, Ricardo Chaves, and Leonel Sousa

- Scalability Study of Polymorphic Register Files
  Catalin Bogdan Ciobanu, Georgi Kuzmanov, and Georgi Gaydadjiev

- Pipelined Large Multiplier Designs on FPGAs
  Ali Senturk and Mustafa Gok

- Implementation Study of FFT on Multi-Lane Vector Processors
  Bogdan Spinean and Georgi Gaydadjiev
DTDS — 2: Dependability and Testing of Digital Systems

Location: Ballroom
Chair: H. Kubátová

- Robust Evaluation of Weighted Random Logic BIST Structures in Industrial Designs
  René Krenz-Baath, Friedrich Hapke, Rolf Hinze, Andreas Glowatz, Reinhard Meier, and Maija Ryynänen

- Test Generation Approach for Post-Silicon Validation of High End Microprocessor
  Satish Kumar Sadasivam, Sangram Alapati, and Varun Mallikarjunan

- Investigating Dependability of Short-Range Wireless Embedded Systems through Hardware Platform based Design
  Benaoumeur Senouci, Anne Johan Annema, Mark Bentum, and Hans Kerkhoff

- Scan Based Tests Via Standard Interfaces
  Christian Gleichner, Heinrich T. Vierhaus, and Piet Engelke

- Soft Error Analysis on Communication Channels in On-Chip Communication Networks
  Mohammadreza Najafi, Saeed Safari, and Zainalabdein Navabi


Location: Gerence 2
Chair: T. Basten

- Virtual Platform for Wireless Sensor Network
  Alvaro Diaz Suarez, Raul Diego, and Pablo Sanchez

- Energy-Aware FPGA-Based Architecture for Wireless Sensor Networks
  Paolo Roberto Grassi and Donatella Sciuto

- Tacit Consent: A Technique to Reduce Redundant Transmissions from Spatially Correlated Nodes in Wireless Sensor Networks
  Paolo Roberto Grassi, Ivan Beretta, Vincenzo Rana, and Donatella Sciuto

- A Predictor-Based Power-Saving Policy for DRAM Memories
  Gervin Thomas, Karthik Chandrasekar, Benny Akesson, Ben Juurlink, and Kees Goossens

- Evaluation of an FPGA-based Reconfigurable SoC for All-Digital Flexible RF Transmitters
  Nelson V. Silva, Manuel Ventura, Arnaudo S. R. Oliveira, and Nuno Borges Carvalho

- Design and Implementation of a Circuit for Mesh Networks with Application in Body Area Networks
  Fardin Derogarian, João Canas Ferreira, and Vítor M. Grade Tavares
**APP — 2: Applications of (Embedded) Digital Systems**

**Location:** Gerence 3  
**Chair:** I. Hamzaoglu

- H.264 Mcroblock Line Level Parallel Video Decoding on Embedded Multicore Processors  
  *Elias Baaklini, Hassan Sbeity, and Smail Niar*

- Enhanced Omnidirectional Image Reconstruction Algorithm and its Real-Time Hardware  
  *Abdulkadir Akin, Elif Errede, Hossein Afshari, Alexandre Schmid, and Yusuf Leblebici*

- A Small and High-performance Coprocessor for Fingerprint Match-On-Card  
  *Taoufik Chouta, Jean-Luc Danger, Laurent Sauvage, and Tanik Graba*

- On-Package Scalability of RF and Inductive Memory Controllers  
  *Mario Donato Marino*

- A hardware accelerator for real time simulation of complex neuronal models  
  *Alessandra Majani, Maria Chiara Lorena, Francesco Leporati, and Giovanni Danese*

- Design of High-Speed Viterbi Decoders on Virtex-6 FPGAs  
  *Mário Véstias, Horacio Neto, and Helena Sarmento*

**15:15-17:30 Sessions**

**WiP: SEAA/DSD Work in Progress**

**Location:** Deniz Kızı 3  
**Chair:** K. Klöckner, K.E. Grosspietsch

- Cost-Efficient Resource Allocation for Multi-tier Web Applications in a Cloud Environment  
  *Adnan Ashraf*

- Goal-Business Process Integration through Choreography within Enterprise Architecture  
  *Cahit Gungor*

- Algorithmic vs Architectural Optimizations in a C-Based PLC to FPGA Translation Environment  
  *Christoforos Economakos and George Economakos*

- Measuring Software Engineer Motivation in Globally Distributed Projects  
  *Liva Šteinberga*

- QoS-enabled Middleware for Smart Grids  
  *Abdel Rahman, Alkhavaja, Luis Lino Ferreira, Michele Albano, and Ricardo Garibay*
- A Proposal for Multidisciplinary Software for People with Autism  
  *Eraldo Guerra and Felipe Furtado*

- High Breakdown Voltage and Switching Speed IGBT Design  
  *A. Belous, I. Lovshenko, V. Nelayev, A. Turtsevich, and I. Shelibak*

- Design Methodology for Implementing Multiplexer Based Ternary Logic Circuits Using Carbon Nanotube Field Effekt Transistor (CNFET)  
  *Chetan Vudadha, P. Sai Phaneendra, V. Sreehari, and M.B. Srinivas*

- A Haskell-Based Programming Paradigm for Coarse-Grained Reconfigurable Arrays  
  *Anja Niedermeier, Jan Kuper, and Gerard Smit*

- Visual Exploration of Changing FPGA Architectures in the VTR Project  
  *Konstantin Nasartschuk, Kenneth B. Kent, and Rainer Herpers*

- Design Synchronization after Partial Dynamic Reconfiguration of Fault Tolerant System  
  *Lukas Miculka and Zdenek Kotasek*

- Analysis Approach for Safety Critical Hardware using Neural Networks  
  *M. Schmedes, A. Th. Schwarzbacher, and B. Hoppe*

- Error-Resilient BDDs: A Preliminary Study  
  *Lorenzo Lago, Anna Bernasconi, and Valentina Ciriani*

17:30 – 18:00 Closing  
*Location: Ballroom*